Long Term Stability of YBCO-Based Josephson Junctions*

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***Abstract*— We report on a study of long term aging in three different types of $YBa_2Cu_3O_{7-x}$ Josephson junctions. Junction aging will affect the choices made in integrating this technology with actual applications. The junction types used in this study are (a) Co-doped barrier edge SNS junctions, (b) noble-metal SNS step-edge junctions, and (c) bicrystal junctions which are either unpassivated or passivated *in situ* with a normal metal shunt or an epitaxial insulator. While all the junctions show degradation, for some the long term survival rate is encouraging.**

I. Introduction

High T_C Josephson junctions are the critical components of many superconductive circuits. Technological applications demand junctions that can be reproducibly fabricated and can withstand the rigors of thermal cycling and long term storage. To date, various research groups have developed reliable processing methods for producing high-T_C thin film electronic devices utilizing Josephson junctions based on $YBa_2Cu_3O_{7-x}$ (YBCO) [1]. However, YBCO thin films degrade with exposure to atmospheric water vapor [2,3] and are also susceptible to surface deoxygenation. These critical issues must be addressed in order to produce junctions that are degradation-resistant and oxygen-stable. There are many examples of protective layers applied to YBCO films that improve the films' long term stability. Depending on the application these layers can be metallic or insulating [3,4], and their effect on the YBCO films vary. In contrast, there is little information regarding the use of protective layers on junctions. We have reported on the protective qualities demonstrated by *in situ* metal shunt layers on bicrystal junctions [5] and the use of STO insulating layers to provide similar protection [5,6]. In this study we report on the aging of three different junction types for which we recorded changes in junction critical current (I_C) and in normal resistance (R_N) over several years. The junction types used in this study are: (a) Co-doped barrier edge SNS junctions ("ramp edge"), (b) noble-metal "step-edge SNS" junctions, and (c) bicrystal grain boundary junctions ("BiGBJs"). This study attempts to establish broad trends indicative of junction aging leading to failure or variation of junction parameters beyond those necessary for the desired applications. While we observed changes in junction characteristics with time, in general, these changes were typically much less than 30%.

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II. Experimental

A. *Fabrication Overview*

The junction fabrication techniques are described below. A cross-sectional view of each junction is shown in Fig. 1.

(a) *Ramp Edge:* Co-doped barrier edge SNS junctions [Fig. 1a].
We present the results of a single chip with 18 junctions of nominal 3 µm width. The SNS edge junctions [7] were grown with off-axis rf magnetron sputtering of the YBCO base electrode and $SrTiO_3$ (STO) base-electrode-insulator bilayer. The ramp edge was patterned by Ar ion milling and cleaned with 100-eV *in situ* Ar ion milling just prior to N-layer deposition. A 10 nm thick $YBa_2Co_{0.21}Cu_2O_x$ N-layer and YBCO counter electrode were also deposited as a bilayer by rf magnetron sputtering. A Au contact layer was deposited *in situ* after counter electrode growth.

b) *step-edge SNS:* Noble-metal SNS step-edge junctions [Fig. 1b].
The step-edge SNS junctions were fabricated by depositing a thin film of YBCO across a step that had been etched into a substrate. Off-axis sputter-deposition was used to produce a film with the c-axis oriented normal to the plane of the substrate. The sharp step-edge produces a break in the superconducting film, exposing a-axis oriented superconductor. The normal metal, either Ag or a Ag-Au alloy, is then *in situ* sputter-deposited such that it covers the step and joins the two superconducting banks. The proximity effect coupling between superconductor and normal metal thus takes advantage of the longer superconducting coherence length afforded by the exposed a-axis oriented material [8,9]. We present the results of five individual chips with seven junctions each of 3, 6, 9 µm width.

(c) *BiGBJs:* Bicrystal grain boundary junctions [Fig. 1c].
The bicrystal junctions were fabricated on commercially purchased [001] oriented STO and sapphire bicrystals with misorientation angles of 24°. A c-axis oriented YBCO film 100 nm thick was deposited with KrF pulsed laser

deposition (PLD). Where an insulating passivation layer was used over the YBCO, it consisted of a 100 nm thick STO layer that was laser ablated *in situ* . Where a normal metal shunt layer was used, it consisted of a dc sputtered Au film of 35 nm thickness deposited *in situ* at 100 °C. The sapphire bicrystal substrate had an initial 20 nm thick CeO_2 buffer layer. Epitaxial, single-orientation growth of all CeO_2 and YBCO layers was confirmed with x-ray diffraction (XRD) analysis. All GBJs were fabricated by patterning microbridges into the YBCO layer using standard photolithography and Ar^+ ion beam etching. The specifics of the fabrication process are described elsewhere [5]. We present the results from one STO-protected bicrystal, and one Au-protected bicrystal. Each sample consists of 14 junctions total, with 7 junctions each of nominal 4 μm and 8 μm widths.

B. *Measurement Issues*

In a study of this nature, involving samples from three separate laboratories, it is necessary to carefully document the conditions underwhich the samples were (i) stored, (ii) thermally cycled, and (iii) electrically measured, so as to provide a meaningful comparison.

(i) In all cases the chips were stored in dessicators that were regularly exposed to atmosphere when opened. The dessicator environment for the step-edge SNS junctions included an Ar-pressurized atmosphere and for the ramp edge junctions the dessicator was over-pressurized with N_2. All samples were fabricated as described and tested, stored and retested periodically. Sample S92-66 had a photoresist layer applied to it after the first recorded test.

(ii) All measurements were carried out in magnetically shielded liquid He or liquid N_2 Dewars. The sample under test was mechanically clamped to the coldstage of the probe and magnetically shielded before being submerged into the dewar. In the case of the ramp edge junction chip, the sample itself was heat-sunk to the probe coldstage using thermal grease. The temperature difference between sample and thermometer was less than 0.5 K. Where applicable, the temperature was monitored and controlled by a thermometer attached to the coldstage near the sample mount location. The thermometer was periodically calibrated against liquid N_2 and liquid He over the several year time span. The thermometer accuracy was known within 0.1 K. Temperature stability and reproducibility are very important: for example, a difference of 1% in temperature between sample and thermometer could result in a critical current change of 6% for the ramp edge junctions. To prevent water vapor damage, during the warming cycle the probe remained in a positive pressure of He or N_2 gas.

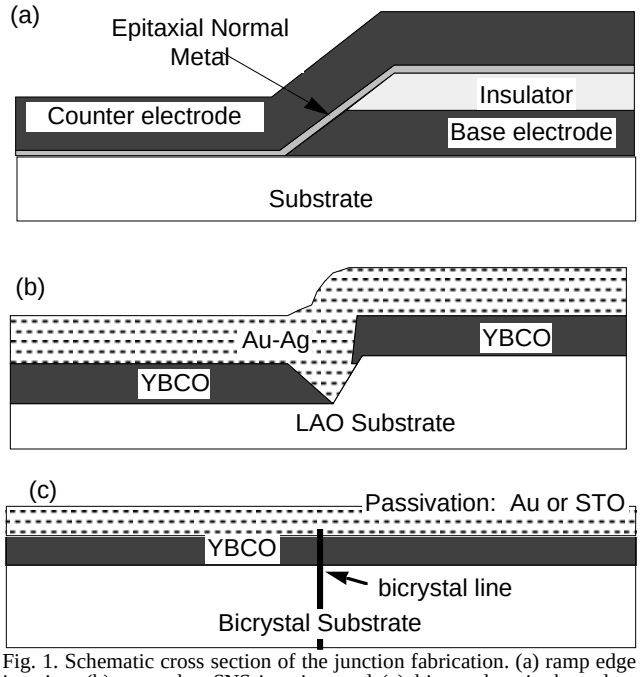

Fig. 1. Schematic cross section of the junction fabrication. (a) ramp edge junction, (b) step-edge SNS junction, and (c) bicrystal grain boundary junction.

(iii) Care must be taken to prevent the trapping of magnetic flux in the junctions and in the superconducting leads. The presence of trapped flux during measurements affects the junction critical currents by applying a magnetic field bias to the Josephson device, leading potentially to as much as a 100% reduction in I_C. To prevent this, the junctions must be cooled in the absence of any magnetic fields. Additionally, it is possible to drive the junction leads into a normal state with too large a bias current, again trapping magnetic flux in the junction. When this occurs the affected junction must be taken above its critical transition temperature and recooled.

III. Results

We reported elsewhere the observation of numerous failures in bicrystal junction samples without any protective layers [5]. On several bicrystal junctions chips, individual junctions with exposed YBCO failed perhaps due to electrostatic sensitivity, environmental exposure, or thermal cycling. These junctions have greater sensitivity to electrostatic discharge, rendering them permanently damaged with regions of high resistivity. Additionally, these unprotected junctions have greater susceptibility to water vapor damage through their exposed surfaces and the exposed grain boundary. In contrast, for the samples presented here from all three sources, no total failures were observed and changes of much less than 25% in junction parameters were typically seen.

In all three laboratories critical currents and normal resistances were measured and archived. The same samples were subsequently remeasured after varying periods of time. Figure 2 is a summary of the on-chip data from (a,b) the ramp edge junctions, (c,d) the step-edge SNS junctions, and (e,f) the BiGBJs. The data shown are for the initial measurement and any subsequent remeasurements of the particular junction set. The I_C and R_N values are normalized to junction width for the step-edge junctions. For the ramp junctions and the BiGBJs they are represented by the critical current density (J_C), and the resistance-area product (R_NA). The I_C and R_N distributions change very little over time; junctions with larger I_C and R_N tend to remain larger at each remeasurement.

Figure 3 is a summary of the data from the samples used in this study. Representative samples were selected for each type of junction, and from two different substrates in the case of the bicrystals. The change in averaged I_C and R_N for all junctions on a given chip is shown relative to its initial measurement. In this manner, a change over time is presented with each subsequent measurement. The junction

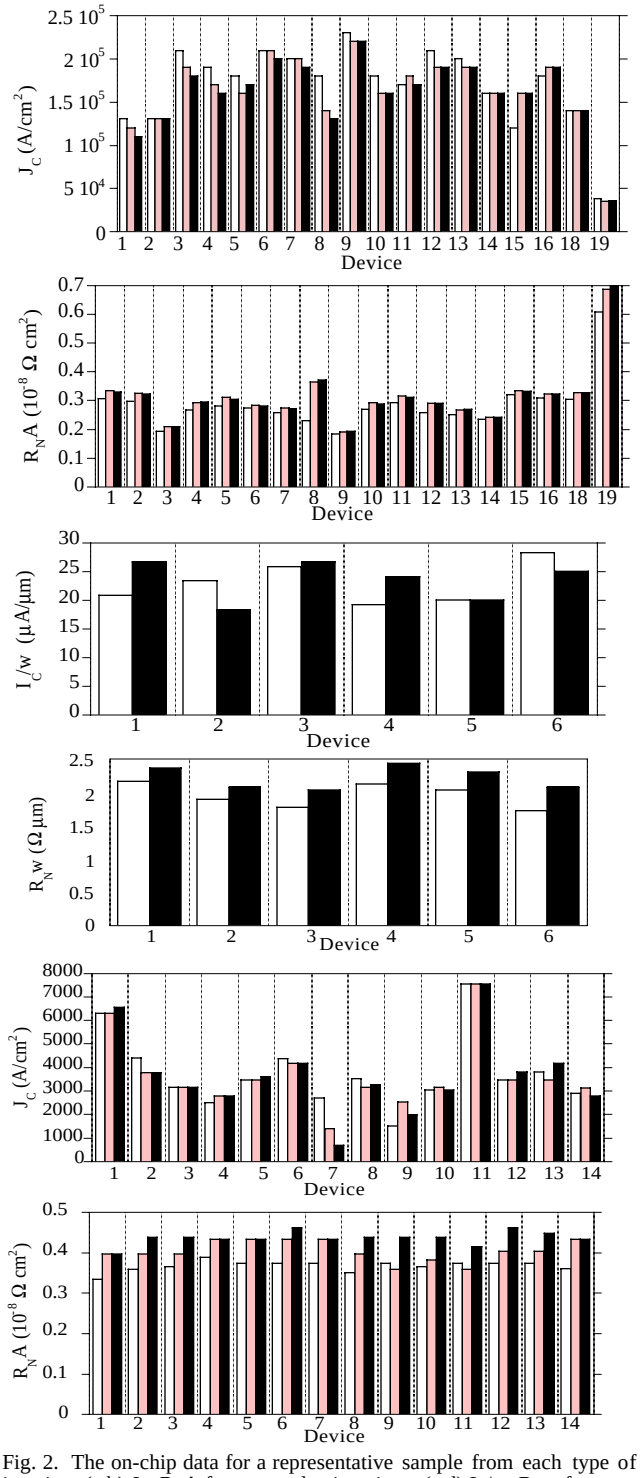

Fig. 2. The on-chip data for a representative sample from each type of junction: (a,b) J_C, R_NA for ramp edge junctions; (c,d) I_C/w, R_Nw for step-edge SNS; and (e,f) J_C, R_NA for BiGBJs. The shaded bar is the original data measurement and the gray bar is the most recent measurement. For 2a,b and 2e,f: the black bar represents an intermediate measurement.

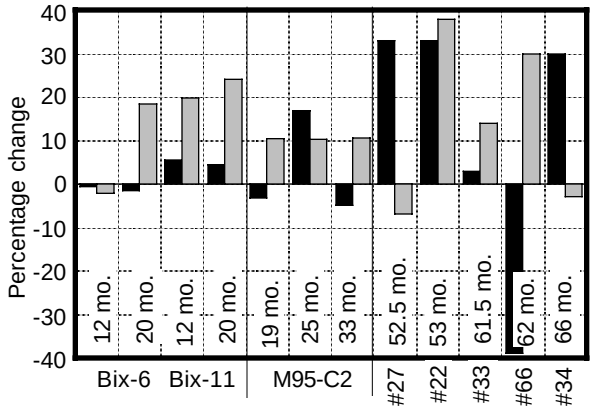

Fig. 3. Percentage change (relative to the initial measurement) in the averaged I_C (black bar) and R_N (gray bar) of all the junctions on a given chip.

measurements spanned as much as 5 years.

Changes in laboratory measurement technique over the time span can cause data measurement variations that introduce systematic errors which make it difficult to put statistically significant error bars on the average measurements at a level better than approximately 5%. Although this is a small sample group, we can use it to identify trends in the data and expose any large deviations from average behavior. In samples from all three groups, the trend in R_N change is positive.

The average changes in I_C are more complex and vary with junction type, measurement reliability, and extrinsic effects such as storage conditions. The ramp edge junctions show a small decrease in I_C as do the BiGBJs on sapphire. The 25 month ramp edge junction measurement (sample C2) shows a large increase in I_C, whereas the 33 month remeasurement shows a small decrease relative to the first measurement. Re-examination of the measurement conditions has revealed that there was poor thermal contact between the sample and the temperature control block, resulting in a temperature difference of 1.8 K. This temperature change caused the shift in I_C shown in Fig. 3, an example of one of the experimental issues discussed earlier. Thus, the ramp edge junction data demonstrate only a small average decrease in I_C. The STO-protected BiGBJs and the step-edge SNS junctions both have an increase of I_C over time. In the case of the step-edge SNS junctions the I_C increase was about 30%, for the STO bicrystal the I_C increase was about 10%.

IV. Discussion

The ramp edge and step-edge SNS junctions in this study had barrier and/or counter-electrode layers deposited *in situ* as part of their junction geometry. In the case of the BiGBJs, additional *in situ* layers of STO or Au were deposited. The vertical structure of the junctions seen in Fig. 1 demonstrate the "self-passivated" nature of these junctions; in all cases the lack of junction surface exposure protects them from more severe degradation. The regions that remain vulnerable to attack are the edges that expose

the ab-planes of the YBCO. Decreases in I_C and corresponding increases in R_N can result if the overall junction cross-sectional areas are decreasing as damage to the YBCO encroaches inward from the edges. Degradation from the edges could be minimized by covering the affected areas with a passivating layer. Care must be taken in choosing the passivation material, since most chemical and thin film processes are also potentially damaging to the YBCO. It is possible that the very large change in sample S92-66 is due to the use of a spun-on photoresist layer left on the chip during its long period of storage.

The junction resistance is independent of sample temperature and insensitive to trapped flux and is therefore a better indicator of changes in the junction over time than is I_C. Increasing R_N trends were observed for all three types of junctions. For the step-edge SNS junctions, the measurement time scale is at least twice as great as that of the other two types represented here. The greater increase observed in R_N for step-edge SNS junctions may be due to their age or to the use of Ag or Ag-Au alloy as the shunting layer. With its greater reactivity, Ag can corrode over time increasing the resistance of the shunting path parallel to the junction interfaces. The ramp edge junctions with an epitaxial oxide normal layer at the interface will not react in this fashion. Similarly, the passivated BiGBJ samples do not incorporate other layers that are sensitive to oxidation or corrosion.

The I_C increases observed in the BiGBJs and step-edge SNS junctions cannot be explained by a simple area loss mechanism and require further investigation. One plausible model for this behavior is the reoxygenation of an oxygen deficient or disordered layer of YBCO at the junction interface. Studying these junctions over very long periods of time would be valuable in estimating such reoxygenation. For the step-edge SNS junctions, the junction interface region is imperfect, resulting in a high interface resistance. We conjecture that, with more initial disorder, these junctions will be more prone to self-annealing, resulting in a larger observed increase in I_C. The ramp edge junction with its epitaxially clean interface exhibits only a small decrease in I_C.

Other experiments that might be explored are junction oxygen anneals. Oxygen plasma anneals performed on ramp edge junctions result in an increase in junction I_C with a small decrease in R_N [10] possibly due to a reversal of junction degradation damage or by encouraging oxygen diffusion to the deficient junction interfaces. Additionally, oxygen electromigration studies [11] may help clarify the significance of oxygen mobility to the long term stability of junction characteristics.

V. CONCLUSIONS

This study of the junction aging effects and stability, demonstrates that these junctions have survived over many years and that they show sufficiently small changes in their characteristics that they can be considered adequate for many applications. Based on an average increase in R_N, these junctions show some degradation in junction characteristics which might be reduced by use of an appropriate passivation layer. Other work has shown that oxygen diffusion contributes to changes in junction critical currents, leading us to speculate that such diffusion could be the factor responsible for the observation of occasional increases in average I_C.

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